24bit serial / parallel converter IC

BU2152FS

BU2152FS is a 24bit serial / parallel converter IC. High-performance output terminal enables LED to be driven directly. Bit numbers can be increased easily by cascade connection.

●Applications

AV equipment such as component stereo, video, and TV
Equipment with built-in micro-controller, and personal computers

●Features

1) LED direct-drive (Output current : 25mA)
2) 24bit parallel output
3) TTL input
4) Low voltage operation (2.7V to 5.5V)
5) Serial data output for cascade connection

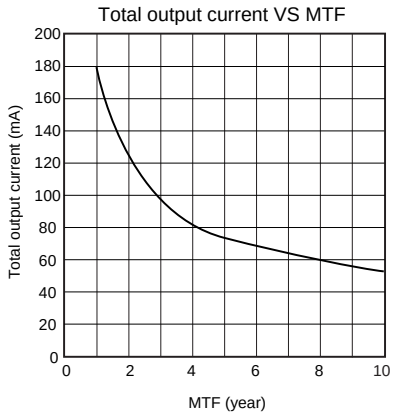
●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{DD}	−0.3 to +7.0	V
Power dissipation	Pd	800∗1	mW
Input voltage	V_{IN}	V_{SS}−0.3 to V_{DD}+0.3	V
Output voltage	V_O	V_{SS}−0.3 to V_{DD}+0.3	V
Total output current	ΣI_O	55 (MAX)∗2	mA
Operating temperature	Topr	−25 to +85	˚C
Storage temperature	Tstg	−55 to +125	˚C

∗1 Decrease 6.4mW per 1˚C when using this IC in Ta=25˚C or above.
∗2 "Total output mean current" is the parameter for reliability, it is given by equation (1).
When MTF is 10 year, ΣI_O become 55mA.

$$1/MTF=\alpha \cdot \Sigma I_O^2 \cdots \text{equation(1)}$$

MTF : Mean Time to Failure (year)
α : a constant (3.306×10^{-5})
ΣI_O : Total output current (mA)

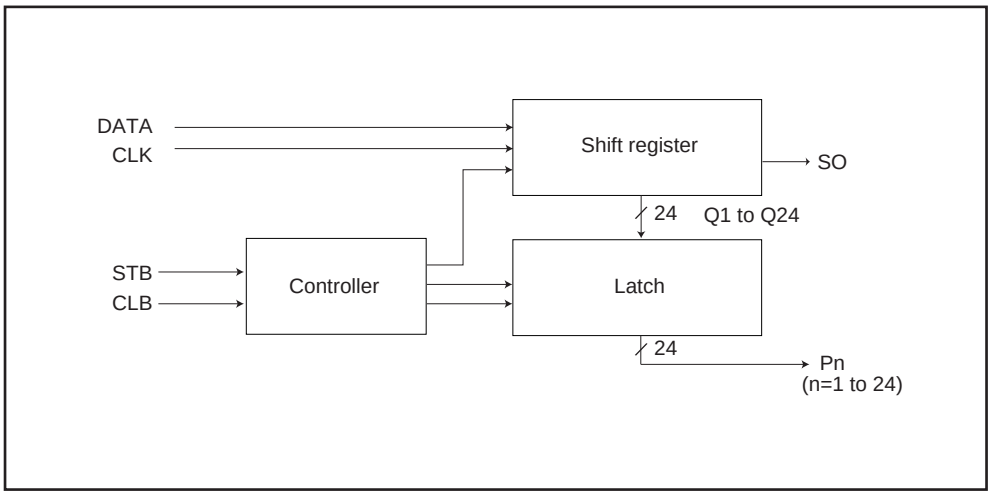


●**Recommended operating conditions** (Ta=25°C, VSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage	VDD	2.7	–	5.5	µA	∗1
Input rise time	tr	–	–	1	µs	applied to CLK, DATA, STB, CLB pins∗2
Input fall time	tf	–	–	1	µs	

∗1 Notes
Set "L" to CLB pin during power up.
Set "H" to CLB pin after power is stable.
When VDD become equal to or less than 2.2V, set "L" to CLB pin to clear the latch circuit.
∗2 Linear transition (without any noise)

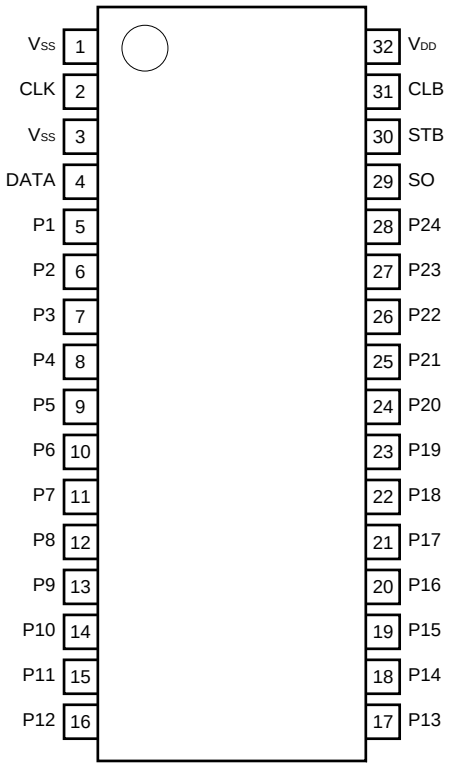
●**Block diagram**



●**Pin descriptions**

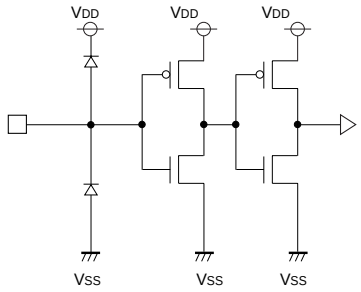
Pin No.	Pin name	Type	Function	Fig.No
1	V_{SS}	–	Ground	–
2	CLK	I	Clock input	A
3	V_{SS}	–	Ground	–
4	DATA	I	Serial input data	A
5	P1	O	Parallel output data	B
6	P2	O		
7	P3	O		
8	P4	O		
9	P5	O		
10	P6	O		
11	P7	O		
12	P8	O		
13	P9	O		
14	P10	O		
15	P11	O		
16	P12	O		
17	P13	O		
18	P14	O		
19	P15	O		
20	P16	O		
21	P17	O		
22	P18	O		
23	P19	O		
24	P20	O		
25	P21	O		
26	P22	O		
27	P23	O		
28	P24	O		
29	SO	O	Cascade output	C
30	STB	I	Input strobe signal active"L"	A
31	CLB	I	Input clear signal active "L"	A
32	V_{DD}	–	Power supply	–

●**Pin assignment**



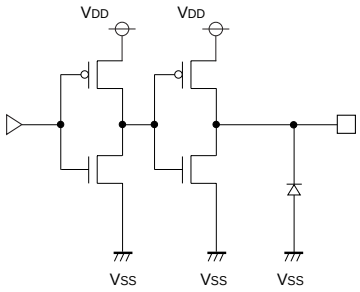
●**I/ O circuitry**

PIN NO.	2,4,30,31



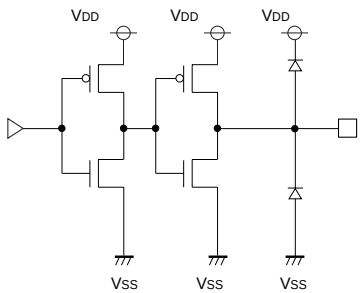
(A)

PIN NO.	5 to 28



(B)

PIN NO.	29



(C)

●**Electrical characteristics**

DC characteristics (Unless otherwise noted, Ta=25°C, V_{DD}=2.7 to 5.5V, V_{SS}=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static current consumption	I_{DDST}	–	–	5	μA	V_{IL}=V_{SS}, V_{IH}=V_{DD}
Input voltage"High" level	V_{IH}	2.0	–	–	V	V_{DD}=5.0V
Input voltage "Low" level	V_{IL}	–	–	0.6	V	V_{DD}=5.0V
Input current "High" level	I_{IH}	–	–	1	μA	
Input current "Low" level	I_{IL}	–	–	1	μA	
Output voltage "High" level	V_{OH}	V_{DD} –1.5	–	–	V	I_{OH}= –25mA
		V_{DD} –1.0	–	–		I_{OH}= –15mA
		V_{DD} –0.5	–	–		I_{OH}= –10mA
Output voltage "Low" level	V_{OL}	–	–	1.5	V	I_{OL}=25mA
		–	–	1.0		I_{OL}=15mA
		–	–	0.8		I_{OL}=10mA

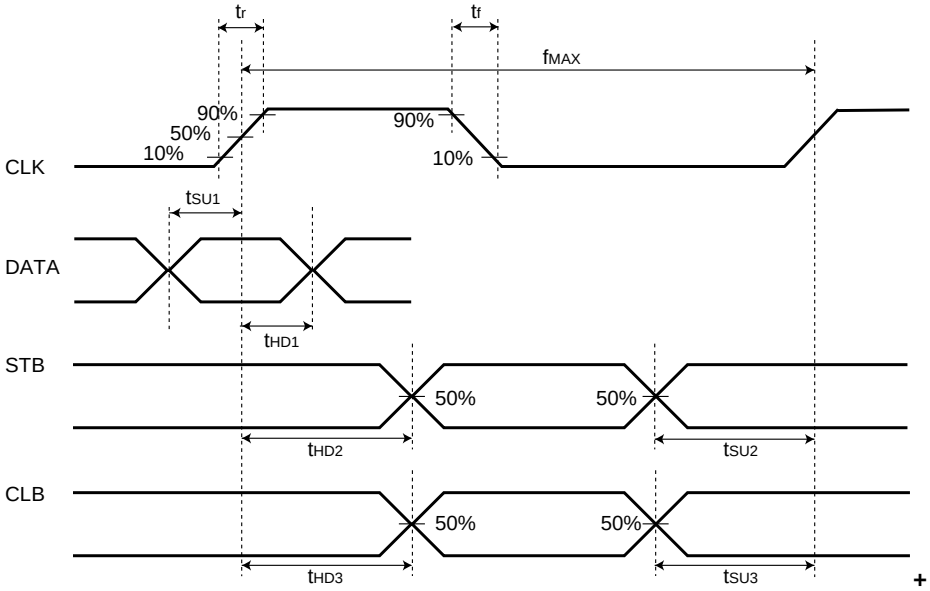
AC characteristics (Unless otherwise noted, Ta=25°C, V_{DD}=2.7 to 5.5V, V_{SS}=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Maximum clock frequency	f_{MAX}	5	–	–	MHz	
Setup time 1	t_{SU1}	20	–	–	ns	DATA to CLK
Hold time 1	t_{HD1}	20	–	–	ns	CLK to DATA
Setup time 2	t_{SU2}	30	–	–	ns	STB to CLK
Hold time 2	t_{HD2}	30	–	–	ns	CLK to STB
Setup time 3	t_{SU3}	30	–	–	ns	CLB to CLK
Hold time 3	t_{HD3}	30	–	–	ns	CLK to CLB
Setup time 4	t_{SU4}	30	–	–	ns	STB to CLB
Hold time 4	t_{HD4}	30	–	–	ns	CLB to STB
Output delay time 1 *	t_{PD1}	–	–	100	ns	CLK to P1 to P24
Output delay time 2 *	t_{PD2}	–	–	80	ns	STB to P1 to P24
Output delay time 3 *	t_{PD3}	–	–	80	ns	CLB to P1 tp P24

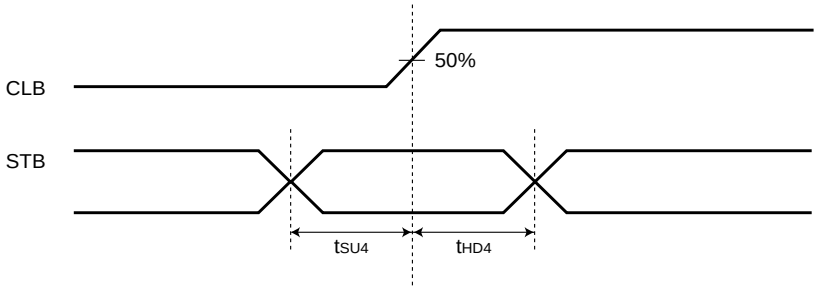
*50pF of load is attached.

• AC characteristic conditions

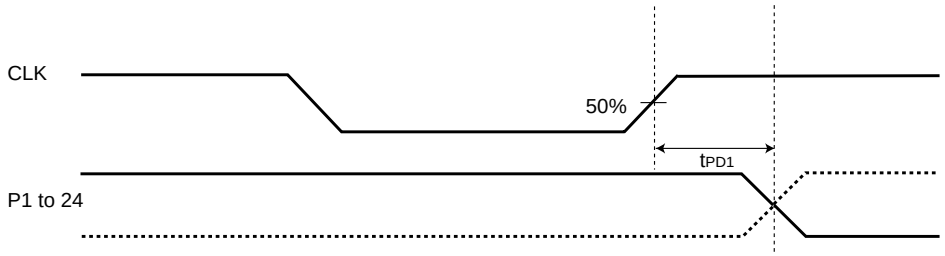
•Setup / Hold time (DATA to CLK, STB t to CLK, CLB to CLK)



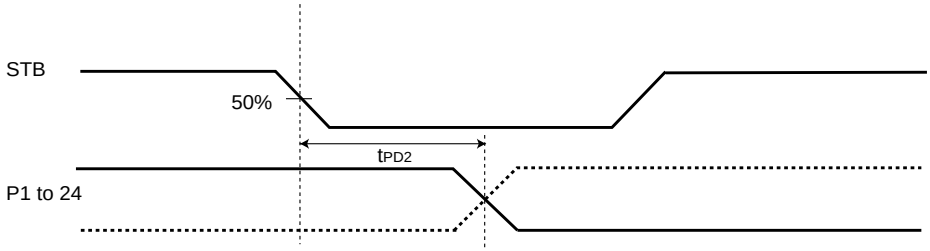
•Setup / Hold time (STB to CLB)



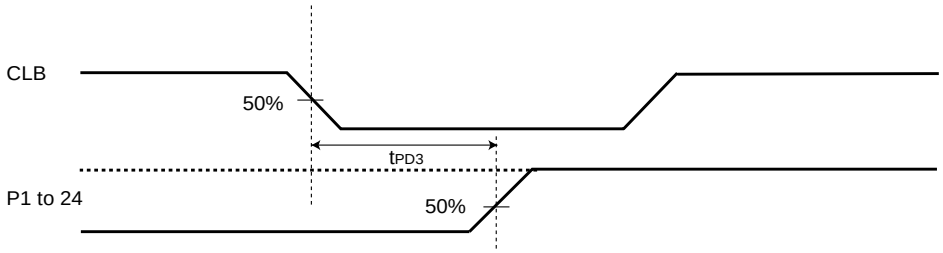
•Output delay time (CLK to P1 to P24)



• Output delay time (STB to P1 to P24)



• Output delay time (CLB to P1 to P24)



●Operating description

(1) Data clear

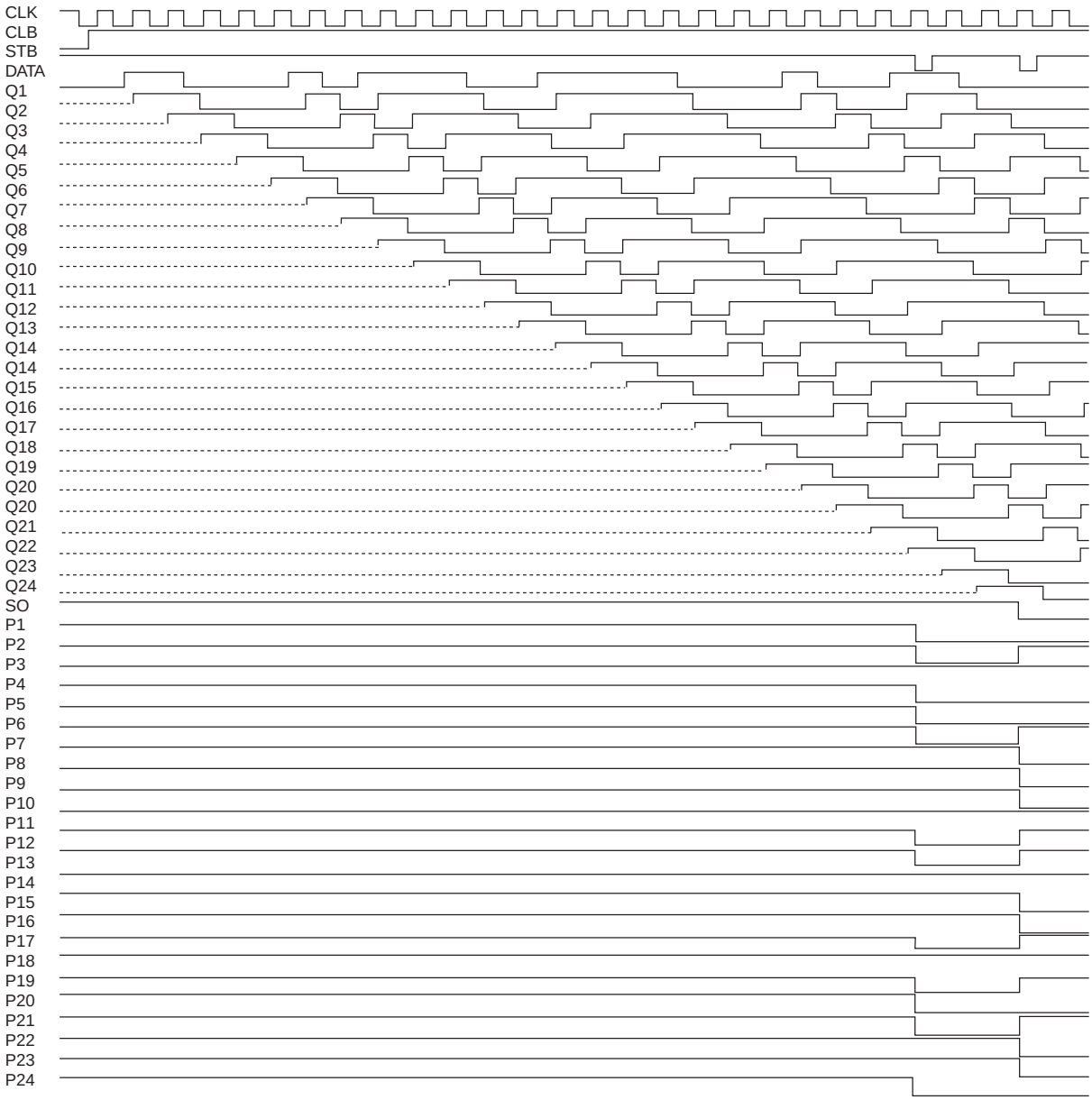
All data of the latch circuit are become “H” when CLB pin is set to “L”, and all the parallel output are become “H”.

(2) Data transfer

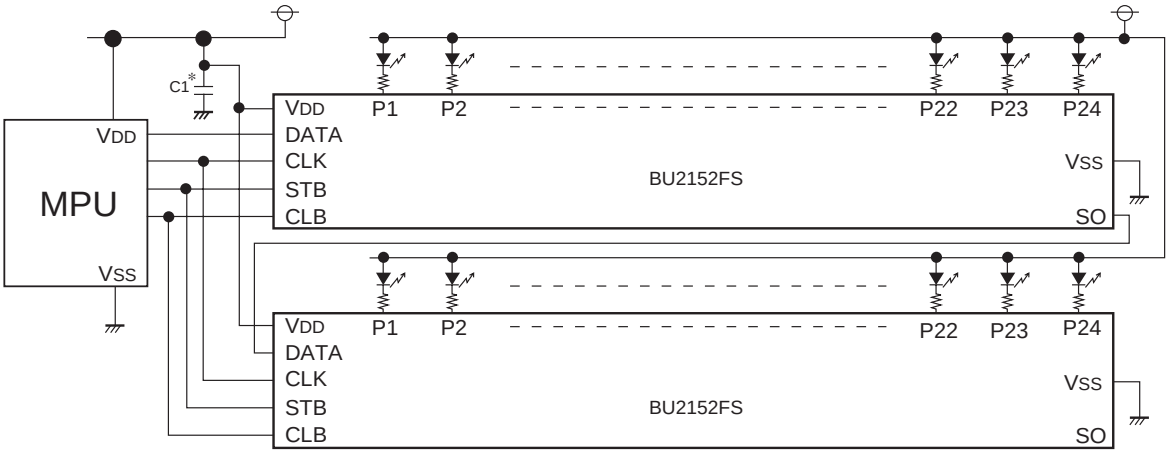
When STB pin is set to “H”, the serial input data of DATA pin is latched to the shift register by the rising edge of CLK pin.
When STB pin is set to “L” after serial data were latched, the data of the shift register are shifted to the latch circuit.

(3) Cascade connection

Serial input data of DATA pin are output through the shift register from SO pin with any conditions of CLB and STB pins.

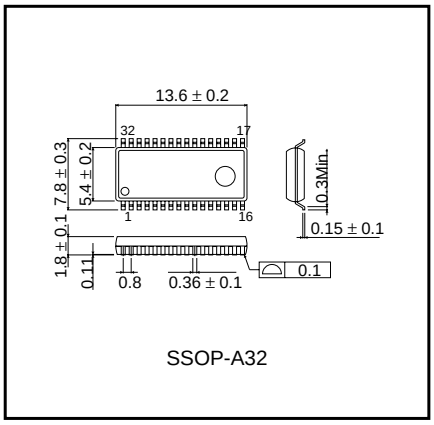


●**Application circuit**



(*Place a capacitor of C1 close to VDD pin as much as possible.)

●**External dimensions** (Unit : mm)



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